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# FIRST SEMESTER M.Sc. DEGREE (REGULAR/SUPPLEMENTARY) EXAMINATION, NOVEMBER 2024

(CBCSS)

**Physics** 

# PHY1C04—ELECTRONICS

(2019 Admission onwards)

Time: Three Hours Maximum: 30 Weightage

#### Section A

Answer all questions.

Each answerable in 7½ minutes.

Each question carries weightage 1.

- 1. Briefly explain the pinch off voltage.
- 2. Briefly explain biasing of FETs.
- 3. Define Population inversion.
- 4. Briefly explain different types of photodiodes.
- 5. Explain Open loop gain.
- 6. Write a short note on dominant pole.
- 7. Briefly explain the shift register using JK flipflop.
- 8. Differentiate between static and dynamic RAM

 $(8 \times 1 = 8 \text{ weightage})$ 

### **Section B**

Answer any **two** questions. Each question carries weightage 5.

- 9. Outline the construction and operation of semiconductor laser.
- 10. Explore closed-loop inverting op-amp configuration, deriving expressions for voltage gain, input impedance, output impedance, and bandwidth.
- 11. Describe the construction and working of a high-pass first order Butterworth filter. Study the frequency response. How is it converted to a second order Butterworth filter.
- 12. Explore the use of shift registers as counters. Discuss the concept of a ring counter and its advantages in specific applications.

 $(2 \times 5 = 10 \text{ weightage})$ 

Turn over

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## **Section C**

Answer any **four** questions. Each question carries weightage 3.

- 13. With diagram and voltage truth table explain MOSFET (negative) NAND gate.
- 14. What is a photoconductor? Obtain the expression for photocurrent.
- 15. Design a differentiator to differentiate an output signal that varies in frequency from 10 Hz to about lKHz.
- 16. Design a second-order low-pass filter at a high cutoff frequency of 1 kHz.
- 17. With the help of timing diagram and truth table explain the working of JK Master Slave flip-flop.
- 18. Describe the characteristic equations of D flip-flop and T flip-flop.
- 19. Using Karnaugh Map solve the given equation to reduce the number of gates used.

$$Y = ABCD + \overline{A}BCD + A\overline{B}CD + AB\overline{C}D + ABC\overline{D}$$

 $(4 \times 3 = 12 \text{ weightage})$