D 131330 **(Pages : 2)** **Name.....**

Reg. No.....

FIRST SEMESTER M.Sc. DEGREE (REGULAR/SUPPLEMENTARY) EXAMINATION, NOVEMBER 2025

(CBCSS)

Physics

PHY IC 04—ELECTRONICS

(2019 Admission onwards)

Time : Three Hours Maximum : 30 Weightage

Section A

Answer **all** *questions.*
Each answerable in 7.5 *minutes.*
Each question carries weightage 1.

1. Draw the circuit of a MOSFET NOT circuit.
2. Sketch a CMOS inverter and explain its operation.
3. Write a short note on the construction and characteristics of a tunnel diode.
4. Briefly explain photo diode and its different types.
5. Briefly explain error currents and error voltage in an operational amplifier.
6. Describe the active low pass filter.
7. Explain JK flip-flop.
8. Briefly explain ring counter.

(8 × 1 = 8 weightage)

Section B

Answer any **two** *questions.*
Each question carries weightage 5.

9. Examine the principle and functionality of a pn junction solar cell. Derive expressions for short-circuit current and efficiency.
10. Explain the closed loop inverting op amp configuration and get the expressions for voltage gain, input impedance, output impedance and bandwidth.

Turn over

11. Illustrate the operation of second order low pass and high pass Butterworth filters using circuit diagrams.

12. With diagram explain the internal architecture of Intel 8085 register organisation.

(2 × 5 = 10 weightage)

Section C

Answer any **four** *questions.*
Each question carries weightage 3.

13. Explain the construction of depletion and enhancement MOSFETs.

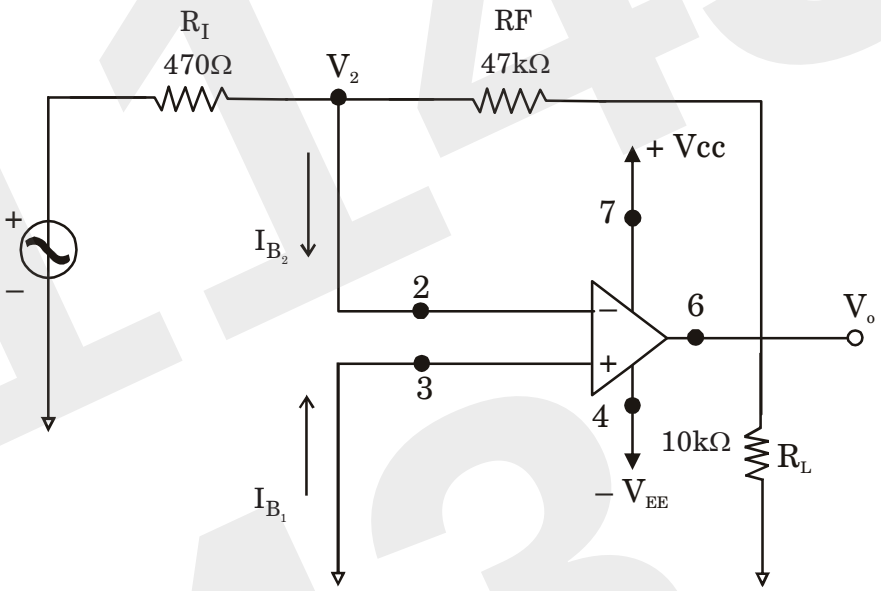
14. For an n-channel silicon FET with a 3×10^{-4} cm and $N_D = 10^{15}$ electrons/cm^3, find (a) the pinch-off voltage and (b) the channel half-width for $V_{GS} = ½ V_P$ and $I_D = 0$.

15. For the inverting amplifier of given figure, determine the possible output offset voltage due to

    (i) input offset voltage V_{io} and

    (ii) input bias current I_B.

    The op-amp is a type 741. V_{io} max = 6mV dc, I_B max = 500 nA dc at $T_A = 25°C$, Vs = ± 15V.



16. Design a low-pass filter at a cutoff frequency of 1 kHz with a passband gain of 2.

17. Sketch the input and output wave forms of a non-inverting comparator with positive and negative reference voltage.

18. Briefly explain synchronous decade counter with the help of a logical circuit diagram

19. Using Karnaugh Map solve the given equation to reduce the number of gates used.

    $Y = AB\bar{C}D + AB\bar{C}\bar{D} + ABCD + \bar{A}BCD + ABC\bar{D} + \bar{A}BC\bar{D}$.

(4 × 3 = 12 weightage)